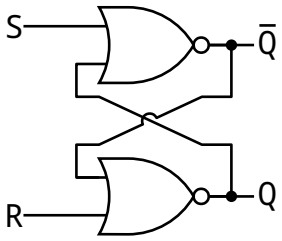
Worksheet: D Latch

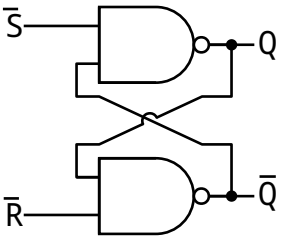
D Latch (Data Latch)

In the last lesson, we learned about the SR latch. We examined an implementation based on NOR gates. There is a similar SR Latch based on NAND gates, but the $\overline{S}$ an $\overline{R}$ inputs are ***active low***, meaning a 0 is considered "true" or "on".

Compare the truth table of these two versions. The invalid state for the active-high (NOR) version is when both S and R are set to 1. The invalid state for the active-low (NAND) version is when both $\overline{S}$ and $\overline{R}$ are both set to 0.

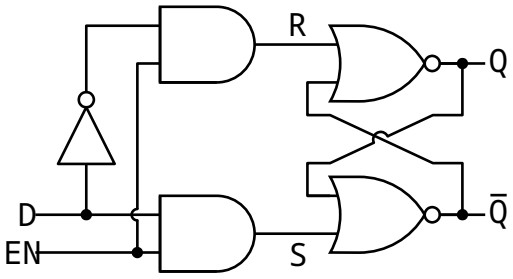


S	R	$\overline{Q}$	Q
0	0	$\overline{Q}$	Q
1	0	0	1
0	1	1	0
1	1	not permitted	



$\overline{S}$	$\overline{R}$	$\overline{Q}$	Q
0	0	not permitted	
1	0	1	0
0	1	0	1
1	1	$\overline{Q}$	Q

In this lesson, we examine an extended version of the SR latch called the D latch. The circuit diagram of a D latch is given below. Notice that the right hand side of the latch is an SR latch. As we have already examined the operation of the SR latch, we need only examine the operation of the left side of the D latch circuit.



EN	D	R	S
0	0		
0	1		
1	0		
1	1		

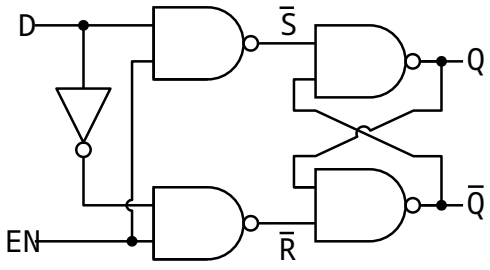
Notice that the circuit can never produce an invalid state for the RS latch.

If the enable line, EN, is set to 0, then both R and S will be always set to 0, and the SR latch will not change state. When EN is set to 1, then:

- when D is 0, R is set to 1, so Q is set to 0.
- when D is 1, S is set to 1, so Q is set to 1.

To say this in a simpler way, while the enable line, EN, is set to 0, the output does not change, and while EN is set to 1, the output follows the input, D.

Note that the circuit can also be implemented using the NAND version of the SR Latch, as shown in the diagram to the right, along with the truth table that applies to both versions.



EN	D	$\overline{Q}$	Q
0	X	$\overline{Q}$	Q
1	0	1	0
1	1	0	1